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| EXAMINER | |
|---|---|
| PUENTE, EVA YI ZHENG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/772,838 | HARDIN ET AL. | |
| | Examiner | Art Unit | |
| | EVA Y. PUENTE | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-6,11-15 and 20-22* is/are allowed.

6)☒ Claim(s) *1,7-10,16-19,23-25* is/are rejected.

7)☒ Claim(s) *26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

*Request for Continued Examination*

1. The request filed on April 18, 2008, for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 10/772,838 is acceptable and a RCE has been established. An action on the RCE follows.

2. Applicant's arguments filed on April 18, 2008 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – (1) Prior art Asano is not a system that reduce the EMI by "spreading" the EMI emission to sideband frequencies. (2) Asano does not teach sideband frequencies.

Examiner's response – (1) Applicant is reminded that the Examiner is entitled to give the broadest reasonable interpretation to the language of claims. The claims recite "a method for reducing electromagnetic emission of data signals". Asano's system comprises a modulation circuit for effectively reduce EMI radiations. The current application and Asano's system both direct to the EMI radiation problems in data transmission and focus to overcome such shortcomings. Applicant's assertion of lacking to teach "spreading" the EMI emission to sideband frequencies was not reflected in claimed language. Asano teaches a method for reducing electromagnetic emission of data signals using a modulating circuit. The modulating circuit may not be operated the same as the instant application. The difference is not recited in the claims. The claim

only requires sideband frequencies that exhibit distinct patterns of electromagnetic energy. (2) The "sideband frequencies" are merely a graphical representation of frequencies other than carrier frequency. Therefore, the claimed sideband frequencies with distinct patterns are interpreted as distinct EMI pattern in the frequency spectrum. As explained before, Asano discloses that EMI radiation is caused by signals with same waveforms and fast repetition rates. The amount of EMI is proportional to the repetition rates. That is, different repetition rates will generate different patterns of EMI energy in the frequency spectrum. The EMI radiation is reduced by EMI modulator that produces signals carried by different waveforms and have waveforms with long repetitive cycles as depicts in Fig. 11B. The EMI modulator produces waveforms with reduced EMI patterns (Col 2, L20-67). Therefore, Asano remove electromagnetic energy by modulating the data signal. Both claimed limitation and Asano achieve at least the same results.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 7, 9, 10, and 16 are rejected under 35 U.S.C. 102(b) as being unpatentable by Asano et al (US 5,793,988).

a) Regarding to claim 1, Asano disclose a method for reducing electromagnetic emissions of data signals, said method comprising:

(a) providing a controller (enable signal in Fig. 2) having a first input (DATA in Fig. 2), a modulating circuit (100 in Fig. 2), and a first output (output of 130, X DATA in Fig. 2);

(b) providing a demodulating circuit (200 in Fig. 2), having a second input (input to block 200 and also the first input to block 220 in Fig. 2), and a second output (output of 230, X DATA in Fig. 2);

(c) providing a data pathway between said first output and said second input (interface cable 30 in Fig. 2);

(d) receiving an input data signal at said first input (DATA in Fig. 2);

(e) repetitively modulating, at said modulating circuit, said input data signal according to a predetermined modulation cycle (counter 110 in Fig.2), in which said modulation cycle comprises at least one modulating pattern set (Fig. 2, 3, and 5 and Col 5, L1-Col 6, L10; counter counts at different time having different pattern, i.e: 0001,0010,0011), thereby generating a first output data signal that is directed to said first output (Fig. 2);

(f) transmitting said first output data signal from said first output to said data pathway (30 in Fig. 2);

(g) receiving said first output data signal from said data pathway at said second input (Fig. 2); and

(h) demodulating, at said demodulating circuit, said first output data signal, thereby generating a second output data signal that is directed to said second output, wherein a

data content of said second output data signal corresponds to a data content of said input data signal (abstract);

wherein said at least one modulation pattern set comprises a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy (According to Asano, EMI radiation is caused by signals with same waveforms and fast repetition rates. The amount of EMI is proportional to the repetition rates. That is, different repetition rates will generate different patterns of EMI energy. The EMI radiation is reduced by EMI modulator that produces signals carried by different waveforms and have waveforms with long repetitive cycles as depicts in Fig. 11B. The EMI modulator produces waveforms with reduced EMI patterns. Col 2, L20-67).

b) Regarding to claims 7 and 16, Asano disclose wherein said controller operates in at least one of a plurality of selectable modes, as follows:

(a) a normal data signal mode without modulation;

(b) a divide by 2 mode without modulation;

(c) a data signal mode with modulation (Col 4, L51-67); and

(d) a divide by 2 mode with modulation.

c) Regarding to claim 9, Asano disclose wherein said controller includes a processing circuit, and said processing circuit comprises one of:

a logic state machine, a sequential processor device, a parallel processor device, and discrete logic elements (N-bit counter in Fig. 2 constitutes as logic state machine or sequential processor device).

d) Regarding to claim 10, Asano disclose a method for reducing electromagnetic emissions of data signals, said method comprising:

(a) providing a controller (enable signal in Fig. 2) having an input (DATA), a modulating circuit (100), and an output (output of 130, X DATA);

(b) receiving an input data signal at said input (DATA);

(c) repetitively modulating, at said modulating circuit, said input data signal according to a predetermined modulation cycle (counter 110), in which said modulation cycle comprises at least two modulating pattern sets (first modulating pattern is counter increments Col 5, L59-Col 6, L2; second modulating pattern is counter decrements Col 6, L27-38) , thereby generating an output data signal that is directed to said output (Fig. 2);

Wherein said at least two modulating pattern sets each comprises a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy. (According to Asano, EMI radiation is caused by signals with same waveforms and repetition rates. The EMI radiation is reduced by EMI modulator that produces waveforms with long repetitive cycles as depicts in Fig. 11B. The EMI modulator produces waveforms with reduced EMI patterns. Col 2, L20-67)

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Ling et al (US 5,977,898).

a) Regarding to claim 8, Asano disclose a demodulating circuit that comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the demodulating circuit comprises one of (a) an exclusive-OR gate, and (b) exclusive NOR gate.

However, Ling et al. disclose an adder circuit comprise an exclusive OR gate (XOR) (410 in Fig. 4). It is well known that an n-bit adder circuit comprises a plurality of logic gates including XOR. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of demodulating circuit of Asano et al with the n-bit adder design of Ling et al. By doing so, provide decision selection and fast response in an n-bit adder.

7. Claims 17-19, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Lo (US 6,026,141).

a) Regarding to claim 17, Asano disclose an electronic controller for reducing electromagnetic emissions of data signals, said controller comprising:

a first input that receives an input data signal (DATA in Fig. 2);

a modulating circuit (100 in Fig. 2), comprising:

a processing circuit that counts a number of transitions of a predetermined type of said input data signal, and that counts a number of repeat cycles of said transitions, and generates a modulation control signal (counter 110, Col 5, L1-Col 6, L39);

a plurality of logic gates that receive said modulation control signal, and said data input signal (adder 120, though not shown explicitly, it is well known that an adder comprises logic gates and multiplexers), and manipulate said data input signal in a manner that generates concentrations of electromagnetic energy emissions near a frequency of said data input signal (abstract; Fig. 11A and 11B), thereby creating a first output data signal (output of 130, X DATA); and

a first output that transmits said first output data signal (output of 130, X DATA and interface cable 30);

wherein the concentrations of electromagnetic energy emissions of said first output data signal comprise a set of sideband frequencies that exhibit distinct patterns of electromagnetic energy. (According to Asano, EMI radiation is caused by signals with same waveforms and repetition rates. The EMI radiation is reduced by EMI modulator that produces waveforms with long repetitive cycles as depicts in Fig. 11B. The EMI modulator produces waveforms with reduced EMI patterns. Col 2, L20-67)

Asano disclose modulating circuit comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the modulating circuit comprises multiplexers.

However, Lo disclose a typical multiple bit counter wherein comprises a plurality of multiplexers (6 in Fig. 3) It is well known that an n-bit counter circuit comprises a

plurality of logic gates including multiplexers. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of modulating circuit of Asano et al with the n-bit counter design of Lo. By doing so, provide fast response and decision in an n-bit counter.

b) Regarding to claim 18, Asano disclose wherein said transition of a predetermined type of said input data signal comprises one of:

(a) a rising edge transition (increments, Col 5, L59-67; Fig. 9); and

(b) a failing edge transition (decrements, Col 6, L27-39; Fig. 9).

c) Regarding to claim 19, Asano disclose wherein a counter element comprises at least one of:

(a) a hardware counter circuit (110 in Fig. 2);

(b) a register that is loaded and unloaded by way of a separate hardware circuit; and

(c) a memory element that is controlled by a processing circuit (120 in Fig. 2).

d) Regarding to claim 23, Asano disclose wherein said processing circuit comprises one of:

a logic state machine, a sequential processor device, a parallel processor device, and discrete logic elements (N-bit counter in Fig. 2 constitutes as logic state machine or sequential processor device).

e) Regarding to claim 24, Asano disclose a receiver circuit having a second input (input to 200 in Fig. 2) and a second output (X DATA in Fig. 2), and a data pathway between said first output and said second input interface cable 30 in Fig. 2);

wherein (a) said data pathway receives said first output data signal from said first output and directs it to said second input, and (b) said receiver circuit demodulates said first output data signal, thereby generating a second output data signal that is directed to said second output, wherein a data content of said second output data signal corresponds to a data content of said input data signal (Fig. 2).

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asano et al (US 5,793,988) in view of Lo (US 6,026,141), further in view of Ling et al (US 5,977,898).

a) Regarding to claim 25, Asano disclose a receiver circuit that comprises an n-bit counter, adder and all the subject matters above except for the specific teaching of wherein the demodulating circuit comprises one of (a) an exclusive-OR gate, and (b) exclusive NOR gate.

However, Ling et al. disclose an adder circuit comprise an exclusive OR gate (XOR) (410 in Fig. 4). It is well known that an n-bit adder circuit comprises a plurality of logic gates including XOR. Therefore, it is obvious to one of ordinary skill in art to combine the teaching of receiver circuit of Asano et al and Lo with the n-bit adder design of Ling et al. By doing so, provide decision selection and fast response in an n-bit adder.

***Allowable Subject Matter***

9. Claims 26 and 27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 2-6, 11-15, and 20-22 are allowed.

11. The following is an examiner's statement of reasons for allowance: None of the prior art teaches or suggests reduce EMI radiation in a communication system, wherein the EMI modulator produces modulation pattern sets. On of the modulation pattern set comprises: counting until a first numeric value for a first repeat cycle; once reach the first numeric value repeat the counting for a second repeat cycle; counting until a number of a plurality of repeat cycles reaches a predetermined second numeric value; and terminate one of the modulation pattern sets.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Puente whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Puente
/E. Y. P./
Examiner, Art Unit 2611

June 5, 2008

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611